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REMARKS

Claims 1-59 are pending in the present application. As an initial matter, Applicants would like to thank the Examiner for allowing claims 8-51 and 56-59.

Claims 2, 3, 7, 53, and 55 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is also a discrepancy in the Office Action regarding Claims 17, 18, and 20. In the Office Action Summary, the Office Action states that these claims have been allowed (No. 5). However, on Page 4 of the Office Action, under Allowable Subject Matter, the Office Action states that "Claims 2, 3, 7, 17, 18, 20, 53, and 55 are objected to as being dependent upon a rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims." Given that Claims 17, 18, and 20 are all dependent upon Claim 16, which has been allowed (Office Action Summary No. 5), Applicants have treated these claims as being allowed. If this is in error, Applicants respectfully request clarification on this issue.

Claims 1, 4-6, 52, and 54 have been rejected under 35 U.S.C. § 102(b) as assertedly being anticipated by U.S. Patent No. 6,069,400 to Kimura et al. (hereinafter "Kimura"). Applicants respectfully traverse this rejection.

Claim 1 recites a method of manufacturing an inter-level dielectric (ILD) that comprises forming an etch-stop layer and three low-dielectric constant material layers. Examples of these low-dielectric constant materials given in the Application all have a dielectric constant below 3.3 (Application, Para. 0024), and generally, any material with

a dielectric constant below that of thermal silicon dioxide (approximately 3.9) is considered to be a low-dielectric constant material (Wolf, Stanley and Richard Tauber, *Silicon Processing for the VLSI Era, Volume 4*, p. 639 (Lattice Press, 2002), included in Appendix A). However, the layers as disclosed in Kimura are all non low-k value dielectrics. Specifically, two of the interlevel dielectric films disclosed in Kimura are TEOS oxide layers, which form a layer of SiO_2. SiO_2 has a k-value of approximately 3.9-4.5, and is not considered to be a low-dielectric constant material. (See *Silicon Processing*, p. 639 in Appendix A). Because Claim 1 explicitly recites low-dielectric constant materials, and Kimura only discloses using high-k value dielectrics, Kimura cannot anticipate Claim 1. Accordingly, Applicants respectfully request that this rejection be withdrawn.

Claim 52 also explicitly recites that the materials to be used are low-dielectric constant materials. As discussed above, Kimura discloses using TEOS oxide for at least two of the layers in its product. TEOS oxide forms a layer of SiO_2, which has a dielectric constant of approximately 4.0. This is not generally considered to be low-dielectric constant material. Accordingly, because the final products have different materials, Kimura does not anticipate Claim 52, and Applicants respectfully request that the rejection to this claim be withdrawn.

In view of the above, Applicants respectfully submit that this response complies with 37 C.F.R. § 1.116. Applicants further submit that claims 1-59 are in condition for allowance. No new matter has been added by this amendment. If the Examiner should have any questions, please contact Applicants' agent at the number listed below. No fee is believed due in connection with this filing. However, in the event that there are any fees due, please charge the same, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

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APPENDIX A

Chapter 14

LOW-*k* DIELECTRICS

For the purposes of IC microelectronic applications, dielectrics are categorized into two classes: 1) *low-k dielectrics* and; 2) *high-k dielectrics*. Those having a dielectric-constant k lower than that of thermal silicon dioxide (i.e., $k < 3.9$) are classified as *low-k dielectrics*, while those having a value higher than that of silicon nitride ($k > 7$), are classified as *high-k dielectrics*. Note that the minimum value of k is 1.0 for air. In this chapter low-k dielectrics are discussed, and in Chap. 4 high-k dielectrics are covered.

14.1 INTRODUCTION TO LOW-*k* DIELECTRICS

Low-k dielectric films are important in advanced IC applications because their use can significantly improve circuit performance characteristics, primarily with respect to interconnect delay. As detailed in Chap. 12, interconnect delay can be reduced not only by decreasing R of the conductor structures in ICs, but also by decreasing C of the dielectric layers (Fig. 14-1). The value of C, in turn, can be reduced by using dielectric materials with smaller permittivity values (i.e., *low-k dielectric materials*).[1] As semiconductor device geometries shrink below 0.25-μm, the parasitic capacitance in the intermetal-dielectric between metal lines becomes more and more important, in terms of the RC-delay in switching.

The primary dielectric film material for interconnects has been SiO_2. The choice of SiO_2 was based on its good dielectric and mechanical strength, as well as its ease of processing. However, SiO_2 has a dielectric-constant ranging from k = 3.9 to 4.5, depending on the method of its formation. This value is too high to be applicable in devices below about 0.18-μm. That is, as indicated in Fig. 14-1 only by using Cu as a conductor together with a low-k dielectric as the insulator, can the sufficiently-low values of RC-delay required for deep-submicron ICs be obtained. Thus, there has been a push to integrate new dielectric materials with k-values smaller than that of SiO_2 into IC fabrication. It should be pointed out that it has become apparent that the tacitly-hoped-for dielectric with $k = 1$ is not realizable, and that some of the qualities of SiO_2 will also no longer be attainable in actual low-k dielectrics. Evaluations of various dielectric materials for low-k thin-film applications will provide the empirical data needed to determine the trade-off limits of k-value versus mechanical performance.